

Description

Introduction

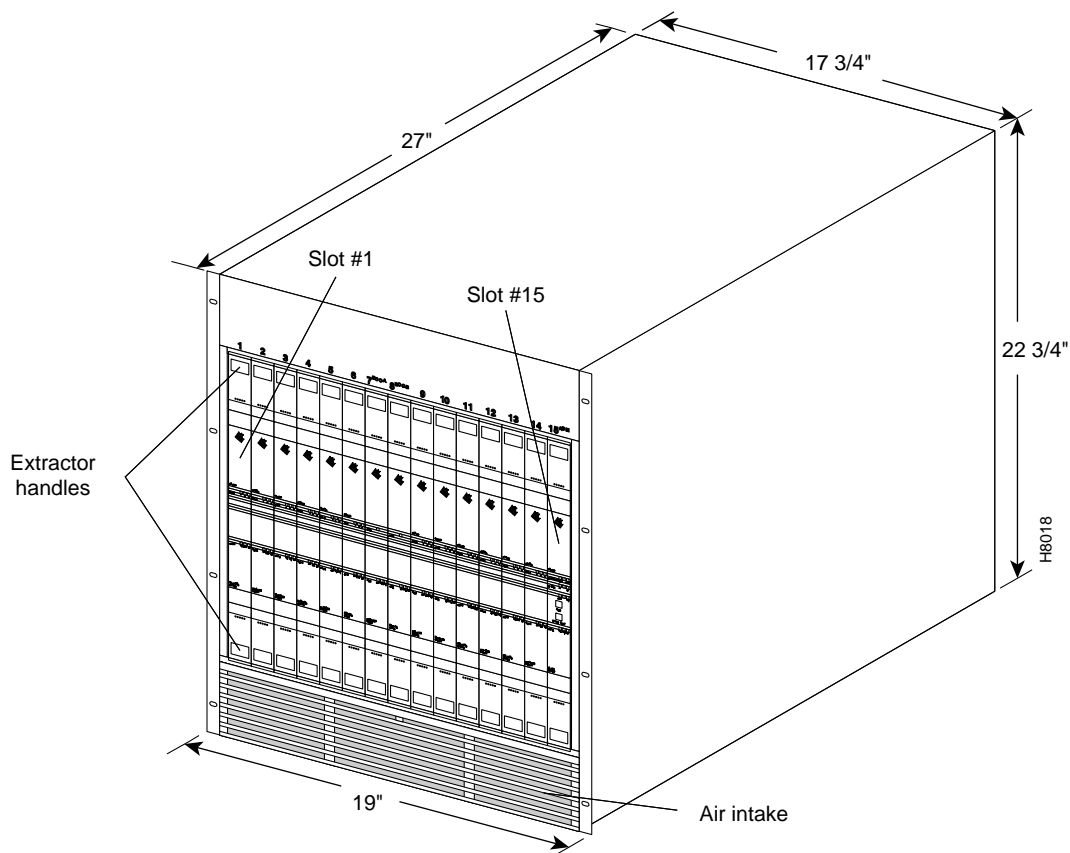
This chapter contains a physical and functional description of the BPX. The physical description includes the BPX enclosure, power, and cooling subsystems. The functional description includes the four major groups comprising the BPX: the Common Core, Network Interface, Service Interface, and Power Supply groups.

Physical Description

The BPX is supplied as a stand-alone assembly. It may be utilized as a stand-alone ATM switch, or it may be integrated at customer sites with one or more narrowband IPX nodes, multi-band IGX nodes, AXIS shelves, and other access devices to provide network access to broadband backbone network links for narrowband traffic. StrataCom and CPE service interface equipment can also be co-located with the BPX and connect to its ATM service interfaces.

BPX Enclosure

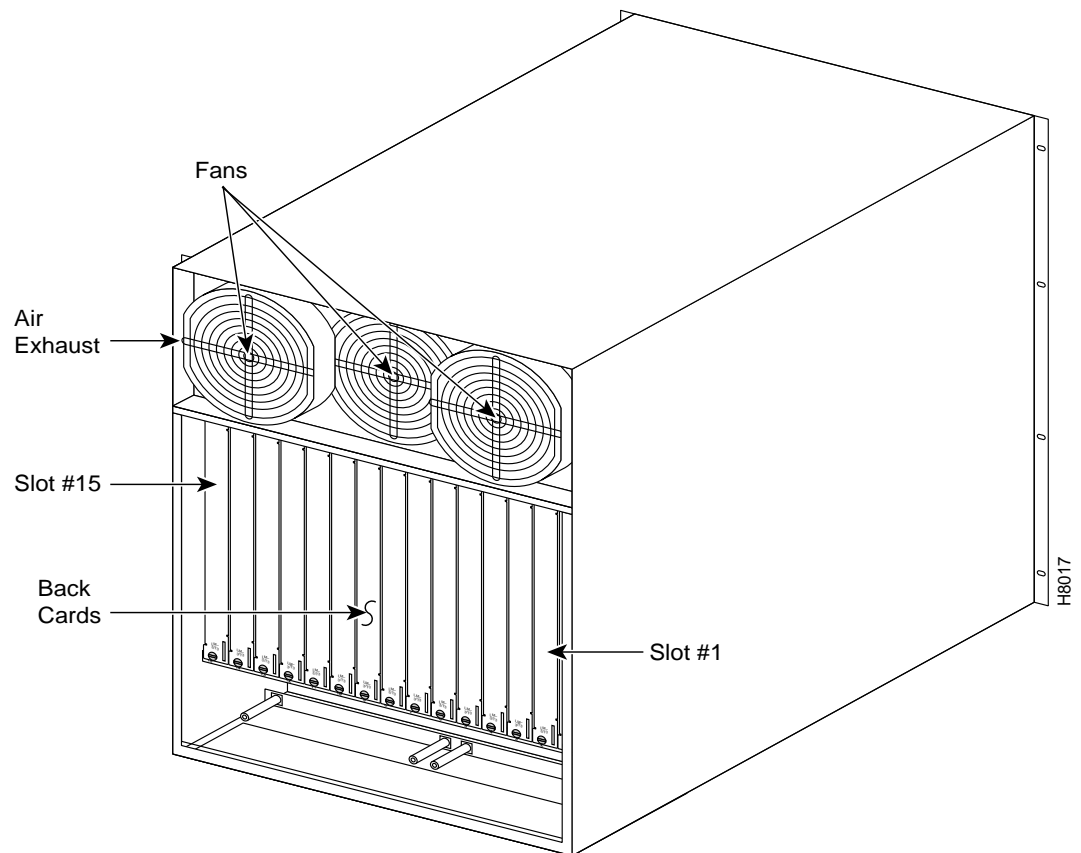
The BPX enclosure is a self-contained chassis which may be rack mounted in any standard 19 inch rack or enclosure with adequate ventilation. It contains a single shelf which provides fifteen slots for vertically mounting the BPX cards front and rear. Refer to Figure 1-1 which illustrate the front view of the BPX Shelf.

Figure 1-1 BPX Cabinet Exterior (Front View)

At the front of the enclosure (Figure 1-1) are 15 slots for mounting the BPX front cards. Once inserted, the cards are locked in place by the air intake grille at the bottom of the enclosure. A mechanical latch on the air intake grille must be released by using a screwdriver and the grille must be tilted forward in order to remove or insert cards.

At the rear of the enclosure (illustrated in Figure 1-2) is another series of card slots for mounting the rear plug-in cards. These are held in place with two thumbscrews, top and bottom. A mid-plane, located between the two sets of plug-in cards, is used for interconnect and is visible only when the cards are removed.

To provide proper cooling, it is essential that blank faceplates be installed in all unused slots. Failure to do so will degrade node cooling and circuit card damage will result. The blank faceplates also provide RFI shielding.

Figure 1-2 BPX Cabinet Exterior (Rear View)

Node Cooling

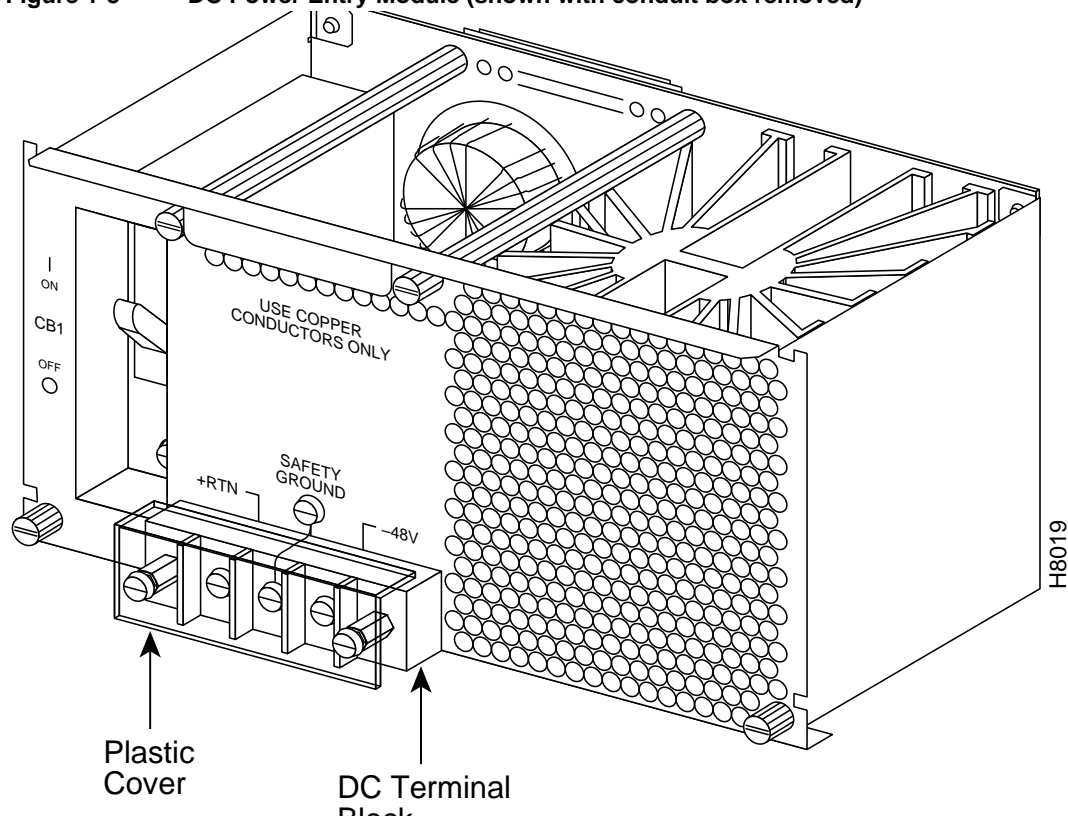
A fan assembly, with three six-inch 48 VDC fans is mounted on a tray at the rear of the BPX shelf (see Figure 1-2). Air for cooling the cards is drawn through an air intake grille located at the bottom in the front of the enclosure. Air passes up between the vertically-mounted cards and exhausts at the top, rear of the chassis. All unused slots in the front are filled with blank faceplates to properly channel airflow.

Node DC Powering

The primary power for a BPX node is -48 VDC which is bused across the backplane for use by all card slots. DC-to-DC converters on each card convert the 48V to lower voltages for use by the card. The 48 VDC input connects directly to the DC Power Entry Module (PEM). The DC Power Entry Module (Figure 1-3) provides a circuit breaker and line filter for the DC input.

Nodes may be equipped with either a single PEM or dual PEMs for redundancy. They are mounted at the back of the node below the backplane. A conduit hookup box or an insulated cover plate is provided for terminating conduit or wire at the DC power input. It is recommended that the source of DC for the node be redundant and separately fused.

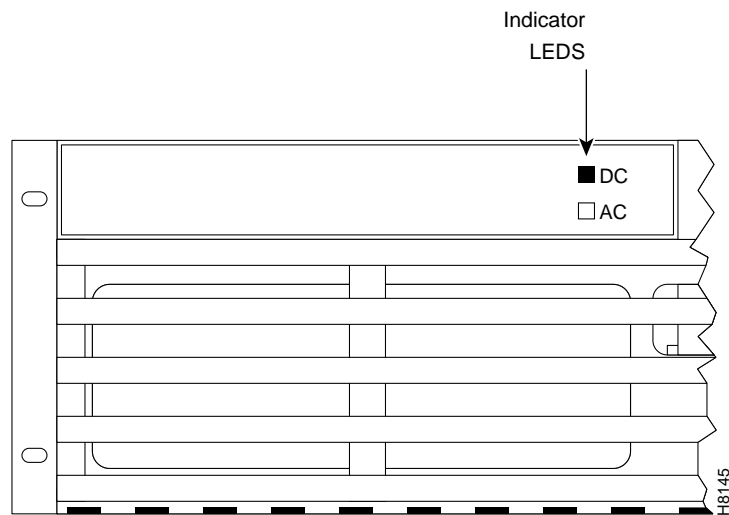
Figure 1-3 DC Power Entry Module (shown with conduit box removed)



Optional AC Power Supply Assembly

For applications requiring operation from an AC power source, an optional AC Power Supply Assembly and shelf is available. It provides a source of -48 VDC from 208/240 VAC input. A shelf, separate from the BPX shelf, houses one or two AC Power Supplies and mounts directly below the node cabinet. This provides a secure enclosure for the power supply assemblies (supplies cannot be removed without the use of tools).

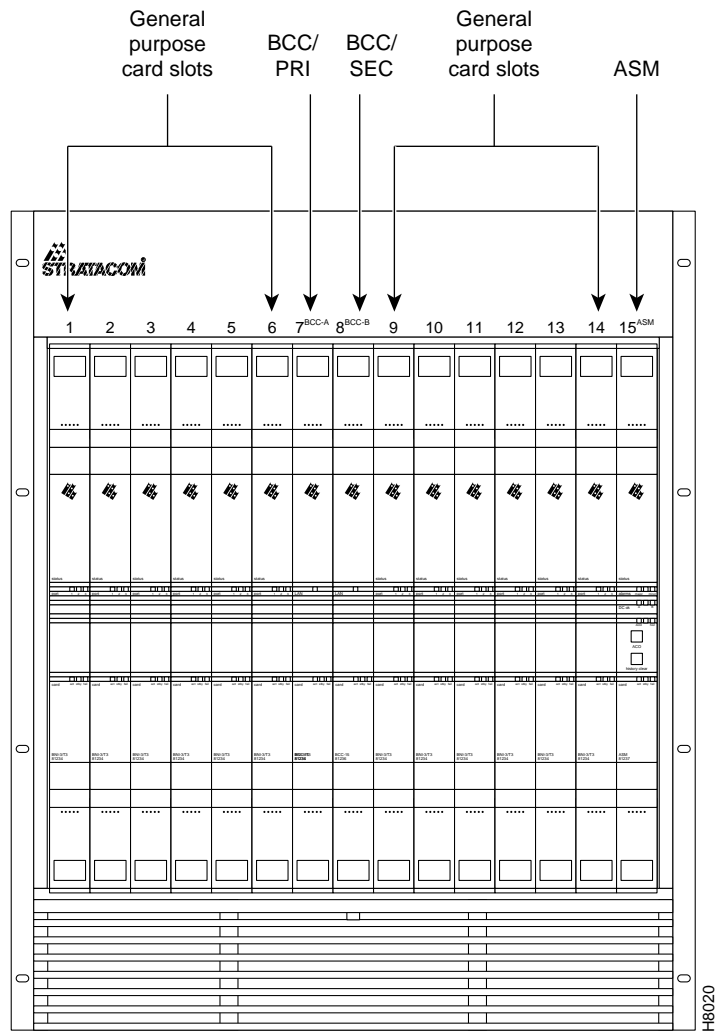
Two of these supplies are usually operated in parallel for fail-safe redundant operation. The front of the AC Power Supplies for the BPX includes two green LEDs to indicate correct range of the AC input and the DC output for each individual supply (see Figure 1-4)

Figure 1-4 AC Power Supply Assembly (Front View)

Card Shelf Configuration

There are fifteen vertical slots in the front of the BPX enclosure to hold plug-in cards (see Figure 1-5). The middle two slots, slots #7 and #8, are used for the primary and secondary BCCs (Broadband Controller Cards). The right-most slot, #15, is used to hold the single Alarm/Status Monitor Card. The other twelve slots, #1 through #6 and #8 through #14, can be used for the Network Interface and Service Interface cards.

Figure 1-5 BPX Card Shelf (Front View)

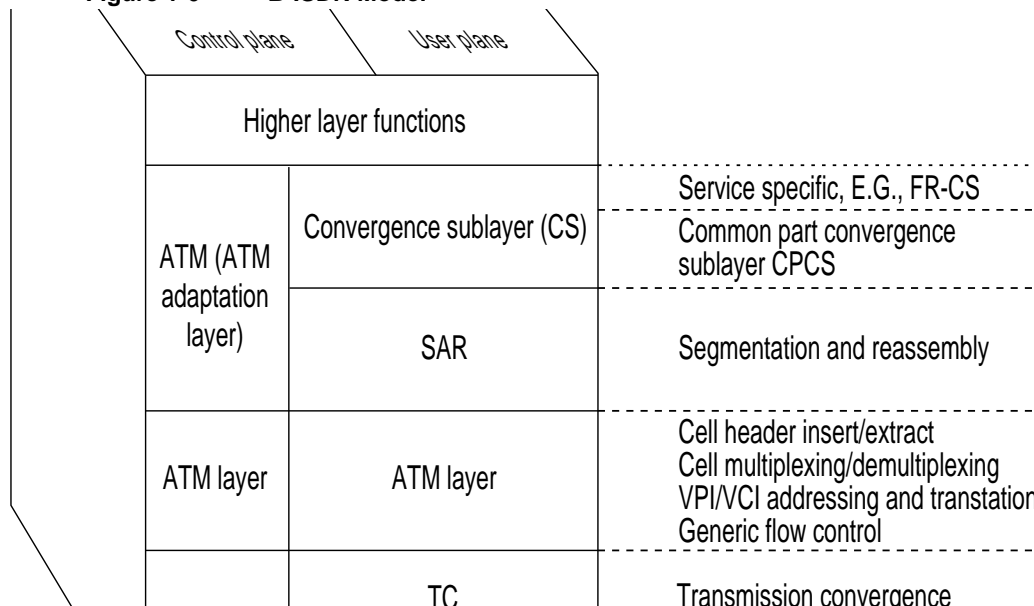


Functional Description

ATM

ATM transmits broadband information using fixed length, relatively small, 53-byte cells which are suitable for carrying both constant rate data (e.g., voice and video) as well as bursty data.

ATM evolved from the Broadband Integrated Services Digital Network (B-ISDN) standard, which in turn is an extension of ISDN. ISDN defines service and interfaces for public telecommunications networks. B-ISDN utilizes a 7-layer reference model similar to the Open Systems Interconnection (OSI) 7-layer architecture. ATM redefines the lower three levels as shown in Figure 1-6. These are the Physical Layer, the ATM layer, and the ATM Adaptation Layer (AAL).

Figure 1-6 B-ISDN Model

Physical Layer

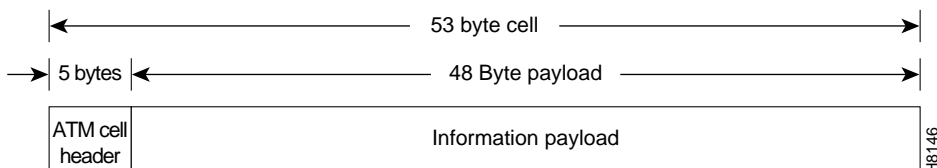
The physical layer is divided into two parts, the Transmission Convergence sub-layer and the Physical Medium sub-layer.

The Physical Medium sub-layer (PMD) handles processing specific to a particular physical layer, such as transmission rate, clock extractions, etc.

The Transmission Convergence sub-layer (TC) extracts the information content from the physical layer data format. This includes HEC generation and checking, extraction of cells from the data stream, processing of idle cells, etc.

ATM Layer

The ATM layer processes ATM cells. The ATM cell consists of a 5-byte header and a 48-byte payload. The header contains the ATM cell address and other management information Figure 1-7.

Figure 1-7 ATM Cell Format

ATM Cell Headers

There are two basic header types defined by the standards committees, a UNI header and a NNI header; both are quite similar. StrataCom has expanded on these header types to provide additional features beyond those proposed for basic ATM service. Usage of each of the various cell header types is described as follows:

- The UNI header (Figure 1-8) must be specified for each *User-to-Network Interface*. A UNI is any interface between a user device, such as an ATM router, and an ATM network.
- The NNI header (Figure 1-9) must be specified for each *Network-to-Network Interface*. This is used, for example, at the interface between a user’s private ATM network and a service provider’s public ATM network.
- The STI header (Figure 1-10) is an extension of these two header types and is a *StrataCom Interface*. This header type is used between StrataCom nodes to provide advanced network features, including ForeSight, that improve performance, efficiency, and congestion control.

Figure 1-8 UNI Header

Bit —	8	7	6	5	4	3	2	1
Byte 1	Flow control				Virtual path identifier			
Byte 2	Virtual path identifier				Virtual circuit identifier			
Byte 3	Virtual circuit identifier							
Byte 4	Virtual circuit identifier				Payload type			Cell loss priority
Byte 5	Header Error Control (HEC)							

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Figure 1-9 NNI Header

Bit —	8	7	6	5	4	3	2	1
Byte 1	Virtual path identifier							
Byte 2	Virtual path identifier				Virtual circuit identifier			
Byte 3	Virtual circuit identifier							
Byte 4	Virtual circuit identifier				Payload type			Cell loss priority
Byte 5	Header Error Control (HEC)							

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Figure 1-10 STI Header**STI Header**

8	7	6	5	4	3	2	1
HCF		VPI					
VPI				VCI			
VCI				Payload class			
CC		F	R	PTI		CLP	
HCS							

HCF: Header Control Field, a 01 indicates an STI Cell
VPI/VCI: Virtual Path/Virtual Channel Identifiers, same as UNI and NNI.

Payload Class:

0001 Non-Timestamped Data/Constant Bit Rate
0010 High Priority/Variable Bit Rate
0011 Voice/Constant Bit Rate
0100 Bursty Data A/Variable Bit Rate
0101 Time-Stamped Data/Constant Bit Rate
0110 Bursty Data B/Variable Bit Rate

CC: Congestion Control

00: No report 10: Congestion
01: Uncongested 11: Severe Congestion

F: Foresight Forward Congestion Indication (FFCI).
Set to 1 if FECN in Frame is a 1, or if incoming cell FFCI is a 1, or egress queue experiences congestion.

R: Reserved

PTI: Payload Type Indicator

CLP: Cell Loss Priority. Same as for UNI or NNI. The CLP bit is set to 1 if the DE is set for a frame, or if the first FastPacket in a frame has its CLP set.

PTI, bits 4,3, and 2:

bit 4 = 0, user data cell;
bit 4 = 1, connection management cell
bit 3 = 0, No congestion experienced
bit 3 = 1, Congestion experienced
bit 2 = 0, for user data cell, indicates CPE information
bit 2 = 1, not used

PTI Bits	Description		
432			
000	User Data Cell	no congestion experienced	SDU Type 0 (CPE information)
001	User Data Cell	no congestion experienced	SDU Type 1
010	User Data Cell	congestion experienced,	SDU Type 0 (CPE information)
011	User Data Cell	congestion experienced,	SDU Type 1
100	Connection Management Cell, OAM F5 Segment Flow Related cell		
101	Congestion Management Cell, OAM F5 End-to-End Flow related cell		
110	Connection Management Cell, reserved for future use.		
111	Connection Management Cell, reserved for future use.		

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The most important fields in all three ATM cell header types are the *Virtual Path Identifier* (VPI) and a *Virtual Circuit Identifier* (VCI). The VPI identifies the route (path) to be taken by the ATM cell while the VCI identifies the circuit or connection number on that path. The VPI and VCI are translated at each ATM switch, they are unique only for a given physical link.

A 4-bit *Generic Flow Control* (GFC) field in the UNI header is intended to be used for controlling user access and flow control. At present, it is not defined by the standards committees and is generally set to all zeros.

A 3-bit *Payload Type Indicator* (PTI) field indicates the type of data being carried in the payload. The first bit is a “0” if the payload contains user information and is a “1” if it carries connection management information. The second bit indicates if the cell experienced congestion over a path. If the payload is user information, the third bit indicates if the information is from Customer Premises Equipment. The PTI field is identical for UNI/NNI/STI.

In the STI header (Figure 1-10), the *Payload Class* is used to indicate various classes of service and BPX queues, e.g., Opticlass, the enhanced class of service feature of the BPX. The *ForeSight Forward Congestion Indication*, the F bit, is used by ForeSight for congestion status.

The *Cell Loss Priority* (CLP) bit follows the PTI bits in all header types. When set, it indicates that the cell is subject to discard if congestion is encountered in the network. For frame relay connections, depending on mapping considerations, the frame Discard Eligibility status is carried by the CLP bit in the ATM Cell. The CLP bit is also set at the ingress to the network for all cells carrying user data transmitted above the minimum rate guaranteed to the user.

ATM Cell Addressing

Each ATM cell contains a two-part address, VPI/VCI, in the cell header. This address uniquely identifies an individual ATM virtual connection on a physical interface. Virtual Channel Indicator (VCI) bits are used to identify the individual circuit or connection. Multiple virtual circuits that traverse the same physical layer connection between nodes are grouped together in a virtual path. The virtual path address is given by the Virtual Path Indicator (VPI) bits. The Virtual Path can be viewed as a trunk that carries multiple circuits all routed the same between switches

The VPI and VCI addresses may be translated at each ATM switch in the network connection route. They are unique only for a given physical link. Therefore, they may be reused in other parts of the network as long as care is taken to avoid conflicts.

The VCI field is 16 bits wide with UNI and NNI header types described earlier. This allows for a total possible 65, 535 unique circuit numbers. The UNI header reserves 8 bits for VPI (256 unique paths) while the NNI reserves 12 bits (4,096 unique paths) as it is likely that more virtual paths will be routed between networks than between a user and the network. The STI header reserves 8 bits for VCI and 10 bits for VPI addresses.

ATM Adaptation Layer (AAL)

The purpose of the ATM Adaptation Layer (AAL) is to receive the data from the various sources or applications and convert, or adapt, it to 48-byte segments that will fit into the payload of an ATM cell. Since ATM benefits from its ability to accommodate data from various sources with differing characteristics, the Adaptation Layer must be flexible.

Traffic from the various sources have been categorized by the standards committees into four general classifications, Class A through Class D, as indicated in Table 1-1. This categorization is somewhat preliminary and initial developments have indicated that it may be desirable to have more than these initial four classes of service.

Table 1-1 Classes of Traffic and Associated AAL Layers

Traffic Class	Class A	Class B	Class C	Class D
Adaptation Layer (AAL)	AAL-1	AAL-2	AAL-3/4 AAL-5	AAL-3/4
Connection Mode	Connection-oriented	Connection-oriented	Connection-oriented	Connectionless
End-to-End Timing Relationship	Yes	Yes	No	No
Bit Rate	Constant	Variable	Variable	Variable
Examples	Uncompressed voice, constant bit-rate video	Compressed voice and video	Frame relay, SNA, TCP-IP, E-mail	SMDS

Initially, four different adaptation layers (AAL1 through AAL4) were envisioned for the four classes of traffic. However, since AAL3 and AAL4 both could carry Class C as well as Class D traffic and since the differences between AAL3 and AAL4 were so slight, the two have been combined into one AAL3/4.

AAL3/4 is quite complex and carries a considerable overhead. Therefore, a fifth adaptation layer, AAL5, has been adopted for carrying Class C traffic, which is simpler and eliminates much of the overhead of the proposed AAL3/4. AAL5 is referred to as the Simple and Efficient Adaptation Layer, or SEAL, and is used for frame relay data.

Since ATM is inherently a connection-oriented transport mechanism and since the early applications of ATM will be heavily oriented towards LAN traffic, many of the initial ATM products are implemented supporting the Class C Adaptation Layer with AAL5 Adaptation Layer processing for carrying frame relay traffic.

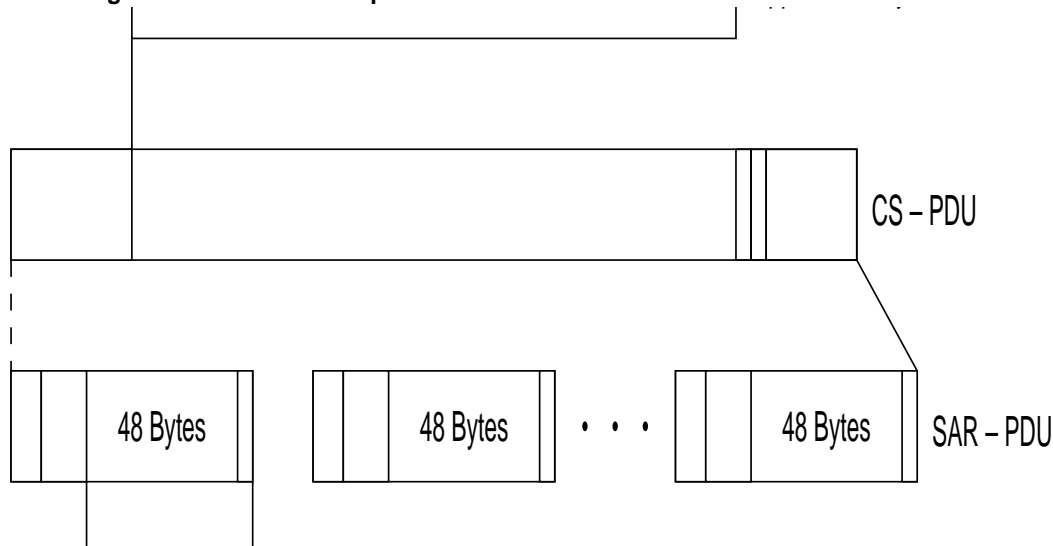
Referring back to Figure 1-6, the ATM Adaptation Layer consists of two sub-layers:

- Convergence Sub-Layer (CS)
- Segmentation and Reassembly Sub-Layer (SAR)

Data is received from the various applications layers by the Convergence Sub-Layer and mapped into the Segmentation and Reassembly Sub-Layer. User information, typically of variable length, is packetized into data packets called Convergence Sublayer Protocol Data Units (CS-PDUs). Depending on the Adaptation Layer, these variable length CS-PDUs will have a short header, trailer, a small amount of padding, and may have a checksum.

The Segmentation and Reassembly Sub-Layer (SAR) receives these CS-PDUs from the Convergence Sub-Layer and segments them into one or more 48-byte SAR-PDUs, which can be carried in the 48-byte ATM information payload bucket. The SAR-PDU maps directly into the 48-byte payload of the ATM cell transmitted by the Physical Layer. Figure 1-11 illustrates an example of the Adaptation Process.

Figure 1-11 SAR Adaptation Process



IPX and IGX Trunk Interfaces to ATM

The IPX/IGX connect to a BPX or other ATM switch via an AIT/BTM T3 or E3 trunk. The AIT(IPX) or BTM (IGX) can operate in several different addressing modes selected by the user (see Table 1-2 and Figure 1-12). To allow the IPX or IGX to be used in mixed networks with other ATM switches, there are two other addressing modes available, Cloud Addressing Mode (CAM) and Simple Addressing Mode (SAM).

BAM

In the BPX Addressing Mode (BAM), used for all StrataCom networks, the system software determines VPI and VCI values for each connection that is added to the network. The user enters the beginning and end points of the connection and the software automatically programs routing tables in each node that will carry the connection to translate the VPI/VCI address. The user does not need to enter anything more. This mode uses the STI header format and can support all of the optional StrataCom features.

SAM

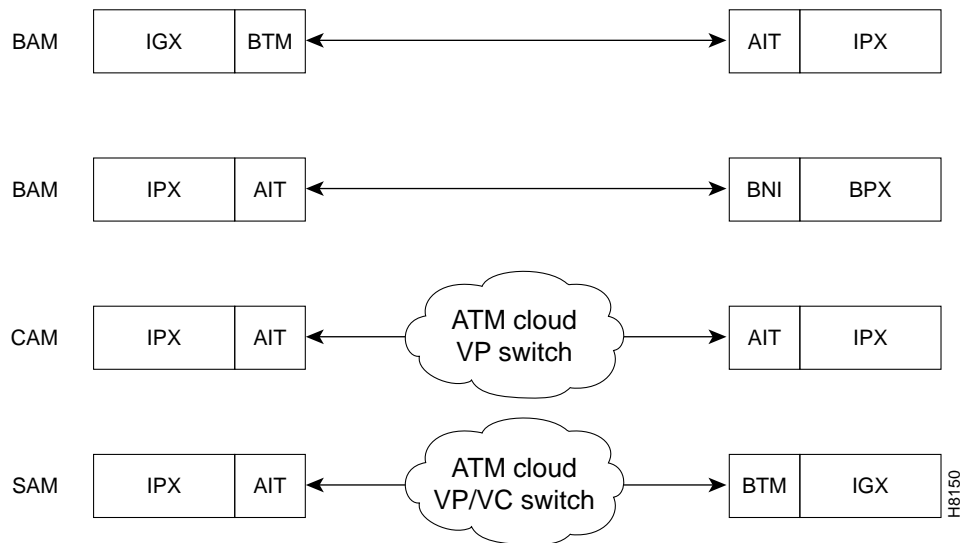
In the Simple Addressing Mode, the user must manually program the path whole address, both VPI and VCI values.

CAM

The Cloud Addressing Mode is used in mixed networks where the virtual path addresses are programmed by the user and the switch decodes the VCI address. Both CAM and SAM utilize the UNI header type.

Table 1-2 ATM Cell Addressing Modes

Addressing Mode	Hdr. Type	Derivation of VPI/VCI	Where Used
BAM-BPX Addressing Mode	STI	VPI/VCI = Node Derived Address	Between IPX (or IGX) and BPX nodes, or between IPX (or IGX) nodes.
CAM— Cloud Addressing Mode	UNI	VPI = User Programmed VCI = Node Derived Address	IPX to IPX (or IGX) connections over networks using ATM switches that switch on VPI only. VPI is manually programmed by user. Terminating IPX converts VCI address to FastPacket address.
SAM— Simple Addressing Mode	UNI	VPI/VCI = User Programmed	IPX to IPX (or IGX) connections over networks using ATM switches that switch where all routing is manually programmed by user, both VPI and VCI.

Figure 1-12 BAM, CAM, and SAM Configurations

Note: IPX with AIT card are interchangeable with IGX with BTM card in this diagram.

FastPacket Adaptation to ATM

A specialized adaptation that is of particular interest to users of StrataCom equipment is the adaptation of IPX FastPackets to ATM cells. There are a large number of narrowband IPX networks currently in existence that are efficiently carrying voice, video, data, and frame relay. A means must be provided to allow these networks to grow by providing a migration path to broadband.

Since FastPackets are already a form of cell relay, the adaptation of FastPackets to ATM cells is relatively simple.

Simple Gateway

With the Simple Gateway protocol, the AIT card in the IPX (or BTM in the IGX) loads 24-byte FastPacket cells into ATM cells in ways that are consistent with each application. (Each of the two FastPacket cells loaded into the ATM Cell is loaded in its entirety, including the FastPacket header.) For example, two FastPackets can be loaded into one ATM cell provided they both have the same destination. This adaptation is performed by the IPX AIT card or the IGX BTM card.

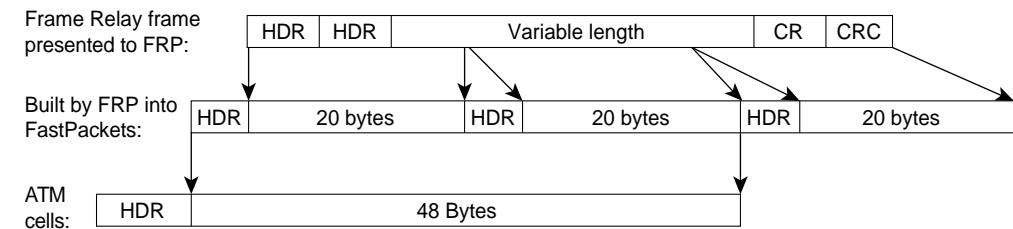
The AIT (or BTM) is configured to wait a given interval for a second FastPacket to combine in one ATM cell for each FastPacket type. The cell is transmitted half full if the wait interval expires. High priority and non-time stamped packets are given a short wait interval. High priority FastPackets will not wait for a second FastPacket. The ATM trunk interface will always wait for frame relay data (bursty data) to send two packets. NPC traffic will always have two FastPackets in an ATM cell.

Complex Gateway, Frame Relay to ATM Network Interworking

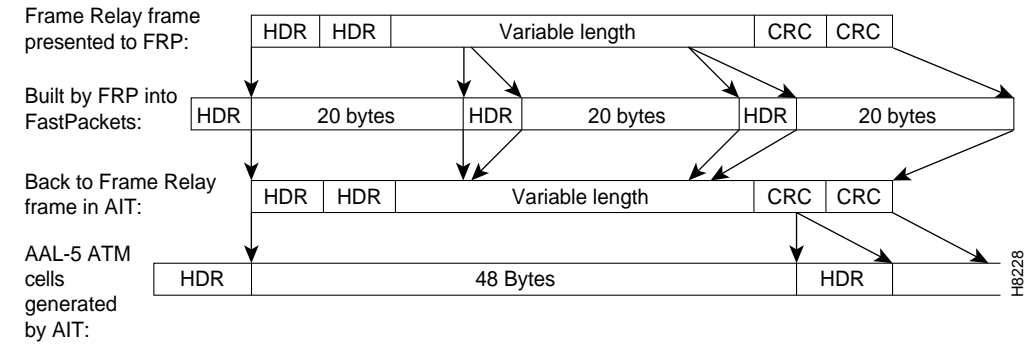
Starting with Release 8.1, with the Complex Gateway capability, the FRSM card in the AXIS, the AIT card in the IPX (or BTM card in the IGX) streams the frame relay data into ATM cells, cell after cell, until the frame has been completely transmitted. Since only the data from the FastPacket is loaded, the Complex Gateway is an efficient mechanism. Also, discard eligibility information carried by the frame relay bit is mapped to the ATM cell CLP bit, and vice versa. See Chapter 13 for further information on frame relay to ATM interworking. A comparison of the simple gateway and complex gateway formats is shown in Figure 1-13.

Figure 1-13 Simple and Complex Gateway Formats

Simple gateway (AIT card) :



Complex gateway (AIT Card) :



BPX Hardware Groups

There are four hardware groups in the BPX. These are listed in Table 1-3.

- Common Core
- Network Interface
- Service Interface
- Power Supplies

Table 1-3 lists the card groups along with a brief description.

Table 1-3 BPX Plug-In Card Summary

Card	Card Name	Where	Model
Common Core Group			
BCC-32	Broadband Controller Card, operates with all versions of System Software Rel. 7.0 and above, and requires 32 Mbyte RAM for 8.1 and later software. For redundancy configuration, installed as a pair of BCC-32s. (System operation equivalent to BCC-3)	Front	
BCC-bc	Back card (also known as LM-BCC) used only with the BCC-32	Back	
BCC-3	Broadband Controller Card, operates with 7.X software versions 7.2.84 and above, and with 8.X System Software versions 8.1.12 and above. For redundancy configuration, installed as a pair of BCC-3s. (System operation equivalent to BCC-32)	Front	
BCC-3-bc	Back card (also know as LM-BCC) used only with BCC-3.	Back	
ASM	Alarm/Status Monitor Card	Front	
LM - ASM	Line Module - Alarm/Status Monitor	Back	
Network Interface Group			
BNI - T3	Broadband Network Interface Card (with 3 T3 Ports)	Front	
LM - 3T3	Line Module - used with BNI-T3 for 3 physical T3 ports. (Configured for 3 ports)	Back	
BNI - E3	Broadband Network Interface Card (with 3 E3 Ports)	Front	
LM - 3E3	Line Module - used with BNI-E3 for 3 physical E3 ports. (Configured for 3 ports)	Back	
BNI-155	Broadband Network Interface Card (with 2 OC3c/STM-1 ports)	Front	
LM-2OC3-SMF	OC3/STM-1 Interface Card, single mode fiber optic, used with either BNI-155 or ASI-155 front card.	Back	
LM-2OC3-SMFLR	OC3/STM-1 Interface Card, single mode fiber optic long range, used with either BNI-155 or ASI-155	Back	
LM-2OC3-MMF	OC3/STM-1 Interface Card, multi-mode fiber optic (1 x 9 LED), used with either BNI-155 or ASI-155 front card.	Back	

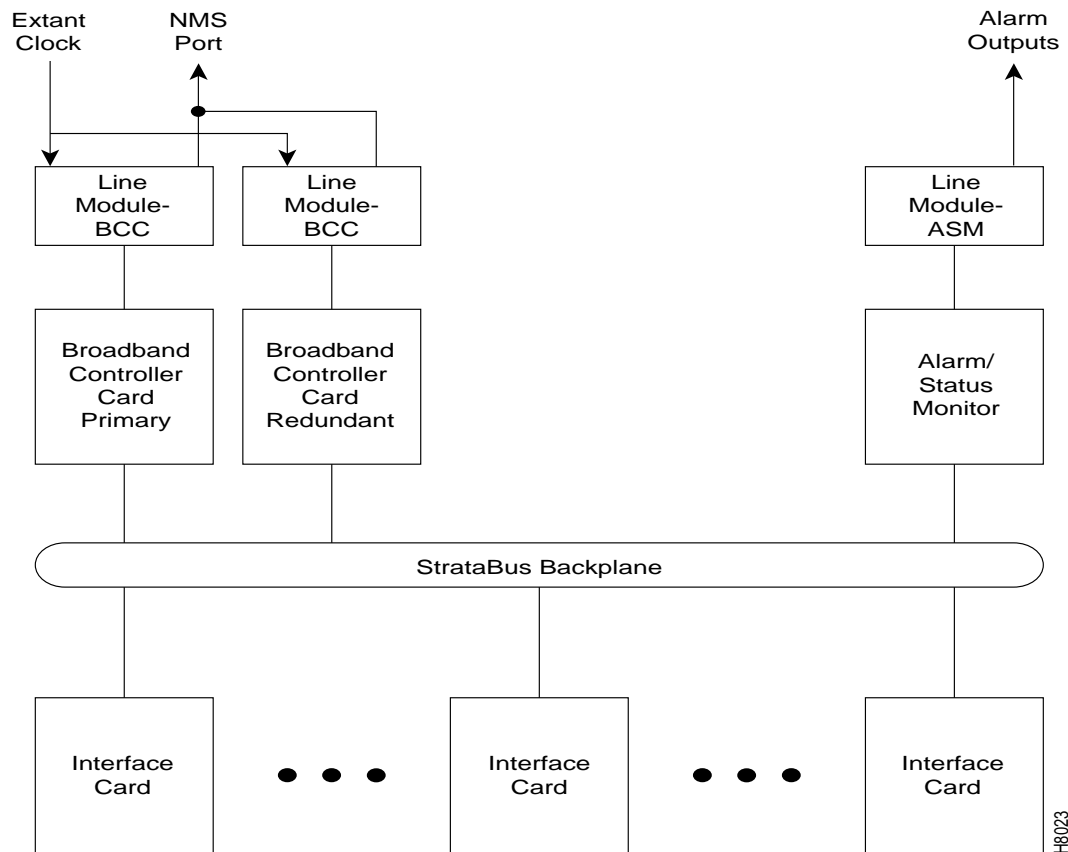
Card	Card Name	Where	Model
Service Interface Group			
ASI-1-2T3	ATM Service Interface Card (with 2 usable T3 ports)	Front	
LM - 3T3	Line Module - used with ASI-1-2T3 for 2 physical T3 ports. (Configured for 2 ports)	Back	
ASI-1-2E3	ATM Service Interface Card (with 2 usable E3 ports)	Front	
LM - 3E3	Line Module - used with BNI-E3 for 2 physical E3 ports. (Configured for 2 ports)	Back	
ASI-155	ATM Service Interface Card (with 2 OC3c/STM-1 ports)	Front	A
LM-2OC3-SMF	OC3/STM-1 Interface Card, SMF (single mode fiber optic) MMF (1x9 LED), used with either BNI-155 or ASI-155 front card.	Back	
LM-2OC3-MMF	OC3/STM-1 Interface Card, multi-fiber mode (1 x 9 LED), used with BNI-155 or ASI-155.)	Back	
LM-2OC3-SMFLR	OC3/STM-1 Interface Card, single mode fiber optic long range, used with either BNI-155 or ASI-155	Back	
Power Supplies			
48 Volt DC Power Supply			
Optional AC Power Supply			

BPX Common Core Group

The BPX Common Core group includes the Broadband Controller Card (BCC-3 and associated BCC-3-bc backcard, or BCC-32 and associated BCC-b backcard), the Alarm/Status Monitor (ASM), a Line Module for the ASM card (LM-ASM), and the StrataBus backplane. The BCC-3 and BCC-32 are functionally equivalent, but use different backcards as listed in Table 1-3. This card group (Figure 1-14) provides the following functions:

- ATM cell switching.
- Internal node communication.
- Remote node communication.
- Node synchronization.
- Network management communications (Ethernet and RS-232).
- Alarm and status monitoring functions

Figure 1-14 Common Core Group Block Diagram



Broadband Controller Card (BCC-3 and BCC-32)

The Broadband Controller Card is a microprocessor-based system controller and is used to control the overall operation of the BPX node. The controller card is a front card that is usually equipped as a redundant pair. Slots #7 and #8 are reserved for the primary and secondary (standby) broadband controller cards, respectively. Each broadband controller front card requires a corresponding back card.

- For non-redundant nodes, either a Broadband Controller Card BCC-3 or BCC-32 is used in front slot number 7.
- For non-redundant nodes, a BCC-3-bc backcard must be used in back slot number 7 with a BCC-3 front card, or a BCC-bc (also known as BCC backcard) must be used in back slot number 7 with a BCC-32 front card.

- For redundant nodes, two Broadband Controller Cards, both BCC-3s or both BCC-32s are used in front slot numbers 7 and 8.
- For redundant nodes, BCC-3 bc backcards must be used in back slot numbers 7 and 8 with BCC-3 front cards, or BCC-c (also known as BCC backcards) backcards must be used in back slot numbers 7 and 8 with BCC-32 front cards.

Note The two types of BCCs with their proper backcards may be operated together temporarily for maintenance purposes, i.e., replacing a failed controller card. Throughout a network, individual BPX nodes may have either a single BCC-3 or BCC-32 controller card, or a pair of BCC-3 cards, or a pair of BCC-32 cards.

For maintenance purposes, e.g., card replacement, the two types of control cards may be temporarily operated together in the same node.

Since the BCC-32 and BCC-3 are functionally equivalent, the term BCC is used in this manual to refer to the functional operation of the Broadband Controller Card. This card group (Figure 1-14) provides the following functions:

Features

The Broadband Controller Card performs the following major system functions:

- Runs the system software for controlling, configuring, diagnosing, and monitoring the BPX node.
- Contains the crosspoint switch matrix operating at 800 Mbps per serial link.
- Contains the arbiter which controls the polling each high-speed data port and grants the access to the switch matrix for each port with data to transfer.
- Generates Stratum 3 system clocking and can synchronize it to either a selected trunk or an external clock input.
- Communicates configuration and control information to all other cards in the same node over the backplane communication bus.
- Communicates with all other nodes in the network.
- Provides a communications processor for an Ethernet LAN port plus two low-speed data ports. The BCC-bc provides the physical interface for the BCC-32, and the BCC-3-bc provides the physical interface for the BCC-3.
- Each Broadband Controller Card includes the following:
 - 68EC040 processor operating at 33 MHz.
 - 32 Mb of DRAM for running system software.
 - 4 Mb of Flash EEPROM for downloading system software.
 - 512 Kbps of BRAM for storing configuration data.
 - EPROM for firmware routines.

- 68302 Utility processor.
- SAR engine processor operating at 33 MHz.
- Communication bus interface.
- HDLC processor for the LAN connection interface.
- Two RS-232 serial port interfaces.

Functional Description

The BPX is a space switch. It employs a crosspoint switch for individual data lines to and from each port. The switching fabric in each BPX node consists of three elements (see Figure 1-15):

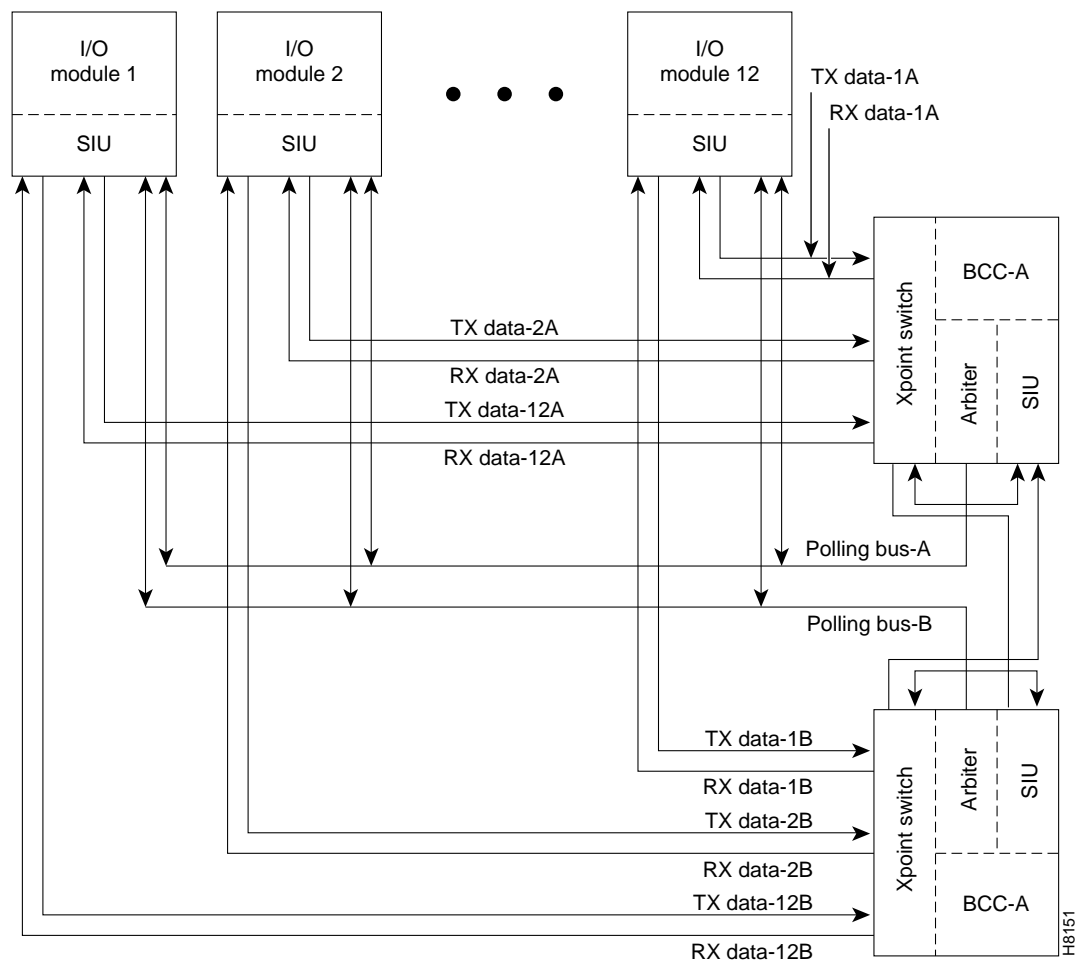
- Central Arbiter on each BCC.
- 16 X 16 Crosspoint Switching Matrix on each BCC (12 X 12 used).
- Serial Interface Modules on each BCC and on each Function Module.

The arbiter polls each card to see if it has data to transmit. It then configures the crosspoint switching matrix to make the connection between the two cards. Each connection is unidirectional and has a capacity of 800 Mbps. (616.7 Mbps for cell traffic plus the frame overhead).

Since there are 16 independent crosspoints and only 15 cards, the switch fabric is non-blocking. However, only one connection at a time is allowed to an individual card. The BPX cell switching is not synchronized to any external clocks; it runs at its own rate. No switch fabric clocks are used to derive synchronization nor are these signals synchronized to any external sources.

Each card contains a Switch Interface Module (SIM) which merely provides a standardized interface between the card and the data lines and polling buses. The SIM responds to queries from the BCC indicating whether it has data ready to transmit.

With the BPX equipped with two BCCs, the cell switching is completely redundant in that there are always two arbiters, two crosspoint switches, two completely independent data buses, and two independent polling buses.

Figure 1-15 BCC Block Diagram

The BCC incorporates non-volatile flash EEPROM which permits new software releases to be downloaded over the network and battery-backup RAM (BRAM) for storing user system configuration data. These memory features maintain system software and configuration data even during power failures, eliminating the need to download software or reconfigure after the power returns.

Node clocking is generated by the BCC. Since the BPX resides as an element in a telecommunications network, it is capable of synchronizing to higher-stratum clocking devices in the network and providing synchronization to lower stratum devices. The BCC can be synchronized to any one of three different sources under software control:

- An internal, high-stability oscillator.
- Derived clock from a BNI module (no IPX clock sources allowed)
- An external clock source connected directly to the BPX.

The BCC clock circuits provide clocking signals to every other card slot. If a function card needs to synchronize its physical interface to the BPX clock, it can use this timing signal to derive the proper reference frequency. These reference frequencies include DS1, E1, DS3, and E3.

Front Panel Description

The BCC (BCC-32 or BCC-3) front panel has four LEDs, three card status LEDs, and a LAN LED. See Figure 1-16 and Table 1-4.

Table 1-4 BCC Front Panel Indicators

No.	Indicator	Function
1.	LAN	Indicates there is data activity over the Ethernet LAN port.
2.	card - act	Card active LED indicates this BCC is on-line and actively controlling the node.
3.	card - stby	Card standby LED indicates this BCC is off-line but is ready to take over control of the node at a moments notice.
4.	card - fail	Card fail LED indicates this BCC has failed the internal self-test routine and needs to be reset or replaced.

The BCC runs self-tests continuously on internal functions in the background and if a failure is detected, the **fail** LED is lighted. If the BCC is configured as a redundant pair, the off-line BCC is indicated by the lighted **stby** LED. The **stby** LED also flashes when a software download or standby update is in progress. The LAN LED indicates activity on the Ethernet port.

Figure 1-16 BCC Front Panel

