AC Extest Meeting
Ft. Collins CO May 21, 2001

Attending:
Ken Parker, Agilent
Benny Lai, Agilent
Mike Gilsdorf, Agilent
Charles Moore, Agilent
Michael Wrightan, Agilent
Richard Lawrence, Agilent
John Rohrbaugh, Agilent
Sylvia Patterson, Agilent
Ted Eaton, Cisco
Bill Eklow, Cisco
Sung Chung, Cisco
Sang Baeg, Cisco
Steven Terry, H-P
Ray Dellecker, JTAG Technologies
Adam Ley, Asset Intertech
Ken Filliter, National Semiconductor
Brad Ishihara, Altera
Brian Sadler, Xilinx
Moises Robinson, Xilinx
Harry Hulvershorn, LogicVision
Bob Russell, EMC
Terry Borroz, Teradyne
Salim Aswat, Solectron
Daljeet Mundae, Mitel
Mike Ricchetti, Intellitech
Carl Barnhart, IBM
Tapan Chakraborty, Lucent
Kevin Nary, W. L. Gore
John Joy, APG Test Consultants, Inc.
George Grant, Anritsu
Dennis Lia, GenRad (via telephone)
Franz de Jong, Philips (via telephone)
Juan Lee, LSI Logic (via telephone)
John Braden, Sun (via telephone)

(Representing end-users, silicon producers, test equipment providers, and other)

Kamran Firooz, VP Agilent, opening remarks. "We don't see any alternative but boundary-scan for digital testing." The themes are miniaturization and high speed. Two challenges:
1. How can we come together for the good of our industry, not our individual companies?

2. What are the roadblocks: technical, licensing, patent issues?

Possible Schedule: (Refer to posting on the website (acextest.org)) Ken Parker is proposing that we work toward IEEE PAR by November 2001. Essentially trying to come to a de facto agreement before going to the IEEE. Why the urgency? Because there are already proprietary silicon implementations under way.

Organization: Can vote if you attend 2 meetings in a row. Lose the vote, if you miss 2 meetings in a row. Selection of officers:
Chair, Bill Eklow
Vice-chair, Carl Barnhart
Editor, Ken Parker
Secretary, Ray Dellecker, interim, for this meeting

Remarks, Bill Eklow, concern is to establish a standard before multiple proprietary solutions are developed. Feels a sense of urgency.

Technical Background:
Review of 1149.1/1149.4 differential treatment. One of the 1149.1 treatments of differential is as 2 separate scan cells, but there are difficulties getting independent control. The analog model calls for cells on the digital side of the converters but it misses continuity faults. 1149.4 has several approaches, including true .4 implementions using the analog TAP. .4 allows measuring the capacitor, but it's time-consuming. Also, at this time, .4 tools and silicon are very limited at this time, brings higher chip costs.

Discussion Point:
1. Objectives: What are we trying to test for? The single ended model is good for finding manufacturing faults: shorts, opens, missing parts. Secondary goal is diagnosis. Question, do we need to detect ac parameter faults? Today, ac-type faults have to be found in functional testing. The test environment will be very different from the mission environment, requiring more difficulty characterizing and controlling the test.

2. High-speed pin design. From the IC design point of view, cannot disturb a high performance output (eg. by tri-stating), but sensing it is sometimes OK.

3. SerDes coding: ac signaling often uses 8B10B coding consisting of some overhead in the mapping of input data stream to what is actually transmitted. But other coding schemes are possible. Today, clocking is usually recovered from the data, instead of separate clock signal.

4. Fault modeling: Sung Chung presented a SPICE-based fault model. (Will be placed on the acextest site) consisting of all of the possible shorts and opens affecting differential drivers. Faults can all be mapped to real defects. Ken Parker presented view of the defect universe, ref slide #19, representing 15 types of ***static*** defects consisting of shorts, opens, and stuck-at's.

Users suggest consideration of a larger, non-static universe. Is it acceptable that boundary-scan verify that construction complies with the netlist, and relying on functional to verify at-speed operation? Users would want scan to do as much at-speed verification as practical because this will reduce the number of test steps. General agreement, we have to be able at a minimum to verify product compliance with the netlist. Some transition faults may get picked up free.

Specific question: is BER testing important?

Proposed Plan:
a. Require detection of static manufacturing faults, consisting of shorts, opens, missing passive devices. (Represents the most commonly seen faults, according to Bill Eklow and agreed by Bob Russell.)
b. Desirable to detect dynamic manufacturing faults, consisting of resistive, wrong values (a. should not exclude b.). ie should be a permission.

Instead of requiring input from the end-users before we start, group's sense is to propose a test method and have them review it.

5. Philips presentation, AC coupled interconnect test using a peak detector, Franz de Jong

Refer to the Philips paper on the website. The resistor may be there as a termination or from the input impedance of the receiver.
In volume production, they see either shorts around the R and C or opens in series with them. Refer to Fig 3 in the Philips paper: proposes a peak detection module, PDM, consisting of a FF with data on the clock input. Looking for signal exceeding threshold at a specific time. The PDM design is not sensitive to different technology implementations.
Question about noise sensitivity, in the differential case. Philips said they had very good experience with one specific design, differentially and single-ended.
Capacitance value in the case of audio was 10 to 100 nf, 100 pf in the case of telecom. Termination resistor was about 250 ohms. They used JTAG Technologies tester at 25 MHz. Only 0 to 1 transitions were tested because it could be tested with a simple peak detector. Use proprietary test software? Yes, they wrote a special cluster test using standard b-scan cells.

6. Criteria to Evaluate the Proposal

Ref. Pages 9-10 in the "Comparison" paper, the initial list of criteria. SerDes designers are pushing the limits, cannot compromise their performance, must be independent of SerDes coding scheme. Scalability/interoperability (eg, capacitor reduction in the range of 4 orders of magnitude)
- Must accommodate coupling capacitors
- Must work for AC/DC boards
- Must work for single-ended and differential
- Must not compromise SerDes performance, independent of the coding scheme, and also for non-SerDes (ie audio) applications

- Must detect/diagnose expected defect spectrum
- Must work in multiple environments (device-to-device, device-to-tester, tester-to-device)
- Must work on common ATE
- Must be independent of SerDes coding scheme
- Must be 1149.1 friendly (use existing tools)
- Must be scalable and interoperable (IC vendors, IC processes, rising frequencies, on-chip capacitors)
- Minimize chip cost/complexity, area, power
- Minimize test cost
- Must be robust (data format, noise susceptibility)
- Must work for functionally valid pairings
- Must be portable/reusable (including any analog circuits)
- Must detect, maximum diagnosis of fault types

7. Cisco MSA Proposal (timing based)

(Posted on the acextest site)

Initial study of the approach was done 12 months ago, working with Cisco's MSA partners. Uses the SPICE fault models presented earlier. The AC pattern is generated at the scan cell. AC and DC tests are done at different TAP state.

Phase-based, 1 and 0 are 180 degrees are out of phase.

Recommends identifying an un-defined logic state (eg a short of the 2 differential signal lines) with null sensor

Three outcomes: Null, Short, AC-status. Need to be identified within the functional domain of the device

Test buffer evolves as the technology evolves because new technology causes new faults

Sample every 16 cycles in RTI

One BSDL for AC and DC

Multiple AC_EXTEST instruction and execution support

Parser will be ready in a month

Features:

- Simple overhead, self contained
- No extra test pin
- Little effort from DC scan design
- Transparent to ATE and CAE tools
- Differential input test buffer filters tester-related CM noise
- No AC interference during DC test
- No need to scale with functional speed and technology changes
- Backward compatible with legacy DC bscan device in DC mode,
- Runs either AC, DC, or both during test

References from TI, Maxim and the IEEE XAUI group are posted in the Cisco paper.

Cisco fault analysis for LVDS using the SPICE model (this presentation will be added to the website):

8 open and short fault classes. 6 are detected by an AC test, and all 8 by AC + DC testing

8 other stuck-at classes. 6 may or may not be detected, depending on the stuck-at voltage level.

8. Patent and IP discussion

Patent has been filed by Cisco. Expect that eventually, a standard will be established. Cisco would examine any compatibility issues with their MSA arrangements. (Agilent intends to allow any IP needed to use their ac-extest capabilities free.)

9. Agilent AC EXTEST Proposal, Frequency-Based

Doesn't matter if there's a phase difference, so time delays don't degrade the performance. Hence, useful for system-level testing.
Requires a global frequency. Freq can scale as the capacitors evolve to smaller values.
Chip designer must decide which pins on the chip are going to be ac coupled and which aren't.
DC pins will treat AC-EXTEST the same way they behave under 1149.1.
For AC testing, transmits either f0 or f1. Requires 1 scan cell to transmit a differential signal and 2 scan cells to receive a differential signal
Built-in noise immunity. Tolerant of some level of extra or missing pulses.
The existing BSDL has a GROUP attribute that allows correlating a single cell driver to two receive cells.
Scalable over range of frequencies and capacitor sizes.
Have to wait for a period of time for the line to be conditioned (capacitors to charge) before test is valid. With low freq circuits, may have to go into RTI. The BSDL extension would have to define this.
Concern about weaknesses of the timing-based proposal:
- Expecting smaller caps to be used, limiting the scalability
- Noise sensitivity

10. Wrapup

Participants should submit comments to the website.
Seeking a selection among the 3 alternatives or new variations by the June 11 telecon.
The call-in number will be posted on the website. Call will start at 8AM Pacific.