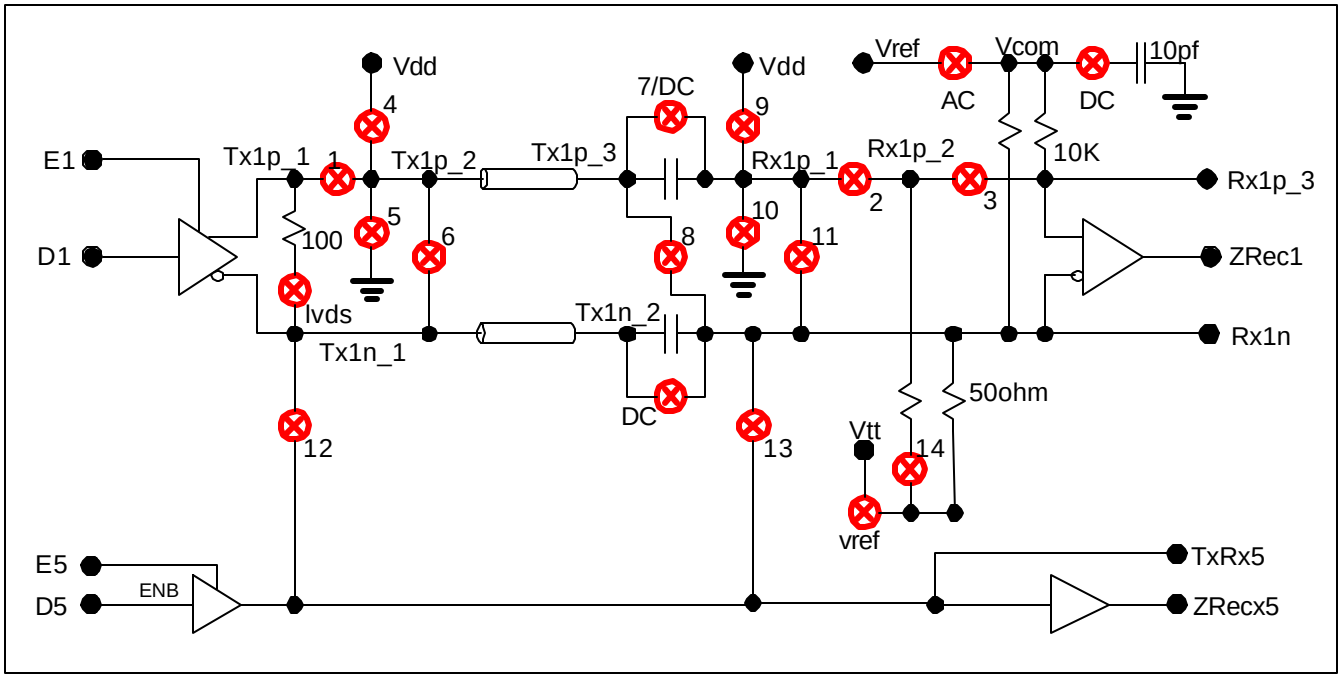
Simulation Model and Nomenclature.



This is the channel model. The coupling capacitors and termination are assumed to be close to the receiver. The red circles are option or defect-injection switches; see the table at right for use. Node terminology is from Adam's Board Tiger Team defect document, substituting p and n for + and -, and allowing for multiple nodes due to potential opens. The transmission line has a delay of 3ns. The coupling capacitors are set according to the formula RC=1/10f for "low frequency", and RC=10/f for "high frequency" simulations. f is currently set to 5MHz (5E6), giving .2nf and 20nf for low and high frequency simulations, respectively. "Vtt" is the termination center tap voltage. "Vref" is the common mode voltage to be set at the receiver when AC-coupled. (For "On-Chip" coupling and termination, the termination resistors connect to nodes Tx1p_3 and Tx1n_2 instead of Rx1p_2 and Rx1n. All circuitry to the right of those nodes is assumed to be on-chip, so defects 2, 3, 7-11, 13, and 14 are deleted.)

The defect and option switch nomenclature is:

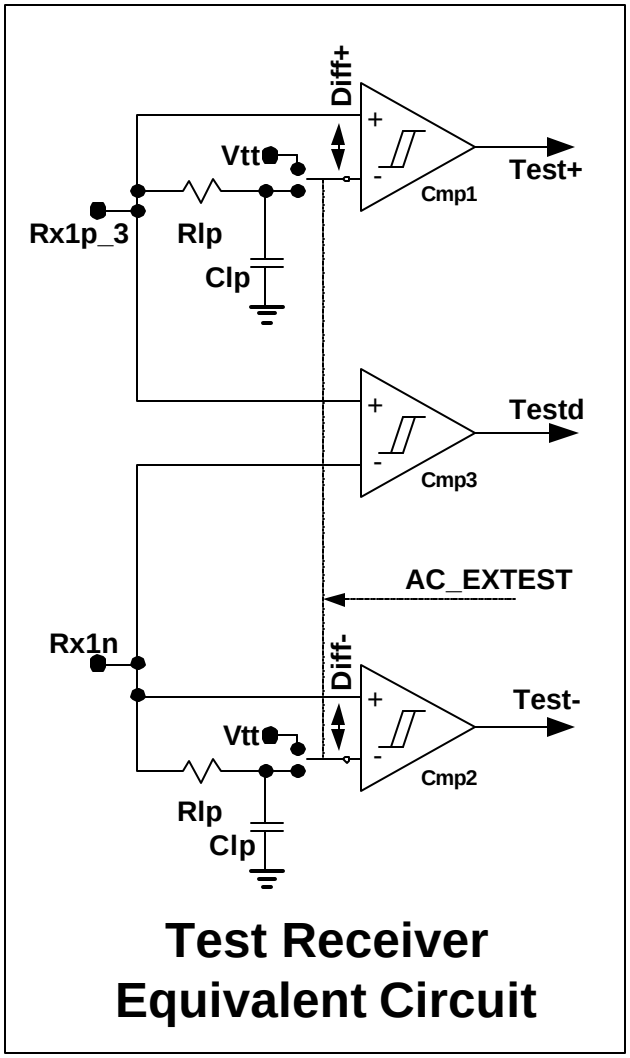
Options:
DC: DC-coupled operation.
AC: AC-coupled operation.
vref: Connect center tap to Vtt.
lvds: source termination, AC-coupled LVDS only.

Opens:
01: Tx1p open.
02: Rx1p open before term.
03: Rx1p open after term.
14: Term+ open/missing.

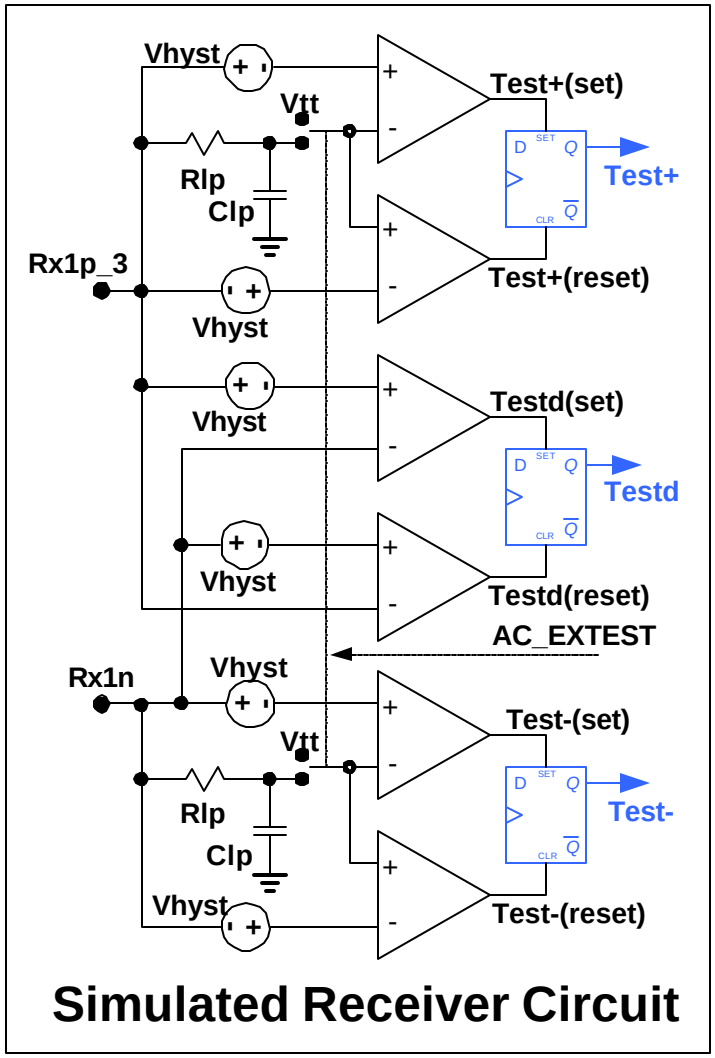
Shorts:
04: Tx1p⇔Vdd.
05: Tx1p⇔Gnd.
06: Tx1p⇔Tx1n.
07: Tx1p⇔Rx1p.
08: Tx1p⇔Rx1n.
09: Rx1p⇔Vdd.
10: Rx1p⇔Gnd.
11: Rx1p⇔Rx1n.
12: Tx1n⇔TxRx5.
13: Rx1n⇔TxRx5.

No Defect:
Simulations with no defect are given defect number 00.

Simulation Model and Nomenclature.



Test Receiver Equivalent Circuit



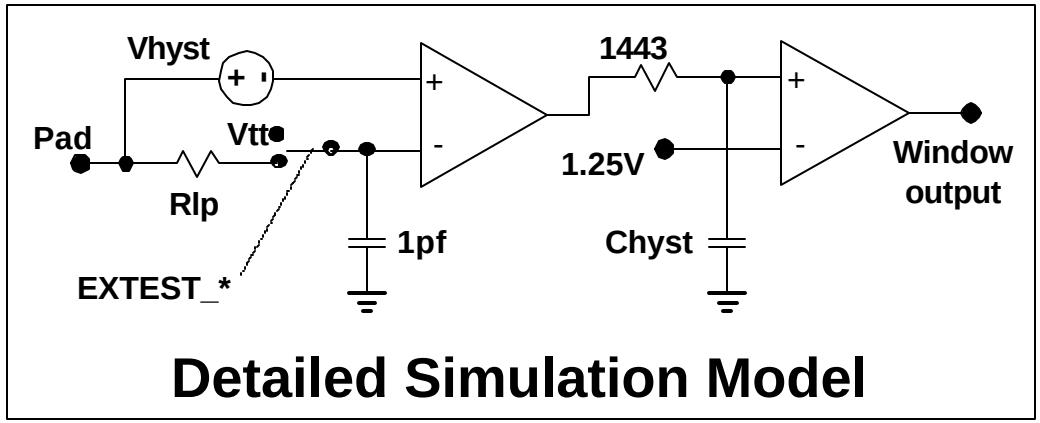
Simulated Receiver Circuit

This shows the test receiver equivalent circuit, and the detailed circuit being modeled with HSpice Voltage-Controlled-Voltage-Source comparators. The second page of the simulation plots show the voltage between the two hysteretic comparator inputs (Diff+, Diff-, and (Rx1p_3 – Rx1n)), coupled with their respective simple comparator outputs:

- Test+(set),
- Test+(reset),
- Test-(set),
- Test-(reset),
- Testd(set), and
- Testd(reset).

The flops and their outputs (in blue) are not modeled or plotted. This allows better evaluation of the selected hysteresis point and of the circuit in general, showing the times that the input was above (set) and below (reset) the hysteresis dead band.

Simulation Model and Nomenclature.



In the Hspice deck:

- The inputs to the first amplifier have various names.
- The output of the first amplifier is named "rawxx".
- The positive input to the second amplifier is named "slewxx".

Where "xx" is one of "ps" (plus-set), "pr" (plus-reset), "ns", "nr" (negative-set and –reset), and "ds", and "dr" (differential-set, -reset).

Further expanding the Test Receiver simulation model, this diagram shows the modeling implementation details of the time hysteresis (Chyst) as well as the voltage hysteresis (Vhyst) and self-reference details (Rlp and 1pf capacitor) for one of the six window comparators. (The switch is down for EXTEST_PULSE or EXTEST_TRAIN, up otherwise.)

To add the time hysteresis, the comparator was split into two amplifiers with a time constant in between. The two amplifiers (Hspice voltage controlled voltage sources) each have a gain of approximately 100, and clip their outputs. The first amplifier has differential inputs and clips its outputs to 1.25+/-1.0V. This gives a delta-V of 1.0 volts between the static output value and the switching point of the next amplifier. The simple RC network has a fixed resistance of 1443 ohms, and the capacitance (Chyst) is varied to change the Thyst value, resulting in 1ns of delay for each pico-farad of capacitance. (As the total swing into the RC network is 2V, the 1V delta-V is 50% of the total swing, which will be reached in .694RC.)

The second amplifier input threshold is at 1.25 volts, and its output clips at ground and Vdd to form a CMOS logic level.

Clearly, this is a simplified and idealized circuit, but it performs the function.