

Russell E. Cummings II

Objective A position in Systems Design and Development requiring my proven abilities in creative problem solving, organization, communication and follow through to provide excellent products and support within given time constraints.

Skills Several designs from concept to production, Schematic entry with Viewdraw/DxDesigner, Mentor Graphics DA, Cadence Orcad (Allegro Design Entry CIS) and Concept (Allegro Design Entry HDL), Cadence Allegro PCB Editor, Cadence Constraint Manager, FPGA design with Altera Quartus II, MAXPLUS II, Verilog, Novas Debussy and Lattice ispLEVER, Documentation with FrameMaker and Word, Debug with Oscilloscope, logic analyzer and DSL test equipment, Programming experience with C, C++ and assembly.

Work experience 7/2004 – Present Freescale Semiconductor Austin, TX

Hardware Engineer

Design of test cards, reference cards and development systems for new PowerQUICC III processors. Tasks included design of system, schematic entry, entry of electrical/layout constraints, direct layout and routing of the PCB, bring-up and debug of the design and support of the design with both internal and external customers. Also designed and implemented several Interposers boards to allow for initial board bring-up before the initial silicon for the new processor was in house. All designs included PCI Express and Serial Rapid IO (SRIO) for high speed serial interfaces, DDR2 memory, local bus sections, multiple Giga-bit Ethernet ports, power-on reset support, I2C interfaces and UART support.

Provided review of customer design based on PowerQUICC III processors including schematic and layout. Also presentations for FAEs and customers along with application and design notes.

Current projects include High-Speed Bridge card to connect two test cards together and allow for testing of multiple PCI Express interfaces, an FPGA design and support of the FPGA to provide a test platform for core exposed test system

4/2004 – 7/2004 Volt, Inc. Austin, TX

Electrical Engineer

Position was a contract Electrical Engineer with Advanced Micro Devices (AMD).

Test and verification of customer designs using AMD processors including the Athlon and Opteron. Testing included HyperTransport and DDR interfaces.

7/2002 – 1/2004 Intrinsity, Inc. Austin, TX

Hardware Application Engineer

I was the hardware applications engineer for the company. Provide support for the 2GHz FastMATH and FastMIPS processors. This includes writing and updating applications notes, customer and new employee training on these parts and support of the evaluation/development board. Was the design engineer for the latest revision of the evaluation board. Documentation is done in Framemaker and Microsoft Office.

My final project is the design of an FPGA to translate a RapidIO port to a PCI Bus. I am also designing the test board for the FPGA, using DxDesigner for schematic entry and will work with a local layout house for the PCB design and manufacturing.

2/2002 – 6/2002 Aerotek, Inc. Tallahassee, FL

Electrical Design Engineer

Position was a contract design engineer with General Dynamics Land Systems. My Project was designing a VME64x backplane for the upgrade of the M1A2 Mission Processor Unit. The backplane includes interfaces to USB, Firewire, Fibre Channel, Ethernet (10BaseT and 100BaseTX), serial ports and 1553 utility bus. This includes schematic entry (DxDesigner and

DxAnalog), writing documentation for the project (Microsoft Office), working with CAD on board layout and design verification.

7/2000 - 5/2001

IBM

Austin, TX

Advisory Engineer

My position was Hardware Applications Engineering providing customer support for the 750CX/CXe PowerPC microprocessor. Responsibilities include answering customer design questions, maintenance of the customer specific and general specifications, writing application notes and validation test plans including schedules for validation.

7/1999 - 6/2000

Cisco Systems, Inc.

Austin, TX

Hardware Engineer

Final project was a re-spin of the Network Interface card for Cisco DSLAMs. This included schematic entry (Viewlogic), component selection, writing hardware functional specifications (FrameMaker and Microsoft Office) and design verification testing. The prior project was the re-design for worldwide use of the Quad CAP/DMT line card. This included schematic entry, component selection, writing hardware functional specifications and design verification testing. This project is now in production. Prior to this I did the final re-spin of the 2 port CAP line card. This project saw limited production and was replaced by the 4 port card. I also work on providing BERT (Bit Error Rate Testing) capability for the 2 port DMT line card. Experience with various chipsets involving Mixed-signal design.

4/1996 - 7/1999

Cisco Systems, Inc.

San Jose, Ca

Hardware Engineer

Design and development of an ATM based ADSL DMT, issue 2 modem. This included schematic entry, PLD design and testing to interface to the motherboard and debug of the design. The PLD was done with Altera AHDL and the MaxPlus II software. Schematic entry was done with Viewlogic. The project was in hardware verification and performance testing at time of transfer to Austin. Experience with various chipsets involving Mixed-signal design.

Design and development of an ISDN-U interface router, the 1604. This included schematic entry, debug and testing to the ANSI T1.601 specification in the lab and at Bellcore. This project took 6 months from start of the System Functional Specification to FCS (First Customer Shipment). There was also the redesign of the 1604 to improve performance and solve problems that arose from the interactions of different Central Office switch types and the MLT (Metallic Loop Termination) circuit. This required several trips to customer sites to gather data and re-testing the fixed units at these sites. The final revision included a Run-From-RAM feature.

Other projects included design of an SDSL WIC (WAN Interface Card) for the 1600 and other platforms, including PLD design, schematic entry and layout. Also took initial schematics for the Micro Web Server from an outside consultant and converted to Cisco standards before the project went to CAD group for layout, including development of symbols for the schematics.

9/1992 - 3/1996

Integrated Device Technology Santa Clara, Ca.

Senior Hardware Application Engineer

Senior Applications Engineer in the RISC Microprocessor Group. Became the group expert for the all 64-bit CPUs including the R4600, R4700, R4000/4400, R4650 and the R5000. Also support all 32-bit CPU and support chips for both the 64 and 32-bit processors. Designed evaluation board for the R4600 and R4650 and designed a module which plugs into the CPU socket for the R5000 with an on board secondary cache. All design projects done with Viewlogic schematic entry tools and netlisters and Altera FPGAs for all system controllers. Also ran Verilog simulations of the R4600, R4700, R4650 and R5000 CPUs to help answer customer and internal questions about the architecture and normal operations. Responsible for teaching and developing sections of the RISC training, writing specifications for new products, providing customer support on the RISC Hotline and design review of customer designs and writing technical users manuals and applications, technical notes and conference papers on the various processors and their use (using FrameMaker and Microsoft Office including PowerPoint). Have also developed code in C, C++ and MIPS assembly to help solve problems for customers and for internal test development.

2/1989 - 8/1992 LSI Logic Milpitas, Ca.

Hardware Application Engineer

Applications Engineer in the MIPS Microprocessor group. Provided support for 32-bit, R3000 based CPU module, the LR33000 32-bit CPU and the 64-bit, MIPS R4000. Also supported 16-bit military 1750A CPU and MMU and development of a CPU core for ASICs based on the L64500 CPU.

Education

1989 - 1994 Stanford University Stanford, Ca.

Masters of Science in Electrical Engineering

1986 - 1989 University Of Illinois Urbana, IL.

Bachelors of Science in Computer Engineering

References

Available upon request